CLAIMS

1. A transistor comprising:

a substrate;

a defined channel region;

a floating gate generally disposed over said channel region separated therefrom by a first insulating layer;

a control gate generally placed on one side of said floating gate separated therefrom by a second insulation layer;

an erase gate generally placed on a second side of said floating gate separated therefrom by said second insulation layer;

a drain region generally disposed on a first side of said floating gate; and

a source region generally disposed on a second side of said floating gate.

2. A transistor as recited in claim 1 wherein said erase gate overlaps said floating gate and said control gate.

3. A method for fabricating a transistor, comprising the steps of:

a) providing a substrate;

b) defining a channel region;

c) growing field oxide in defined areas;

d) providing a first insulating layer;

e) depositing a first poly-silicon layer;

f) defining from said first poly-silicon layer a floating gate generally positioned over said channel region;

g) doping a source region;

h) providing a second insulating layer;

i) depositing a second poly-silicon layer;

j) defining a control gate and an erase gate; and

k) doping a drain region.

4. A method as recited in claim 3 wherein said control gate is generally positioned on a first side of said floating gate and overlapping said floating gate.

5. A method as recited in claim 3 wherein said erase gate is generally positioned on a second side of said floating gate and overlapping said floating gate.

6. A method as recited in claim 5 wherein said erase gate is generally positioned on said second side of said floating gate and overlapping said floating gate and said control gate.

7. A method as recited in claim 5 wherein said erase gate is generally positioned on said second side of said floating gate and overlapping said floating gate and about flush with said control gate.

8. A memory array comprising a plurality of memory cells each having a floating gate, an erase gate, a control gate, a source region, and a drain region comprising:

a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same rows are connected by a common erase line, and the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line; and

control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array.

9. A memory array as recited in claim 8 wherein each of said memory cells comprising: a substrate, a defined channel region, a floating gate generally disposed over said channel region separated therefrom by a first insulating layer, a control gate generally placed on one side of said floating gate separated therefrom by a second insulation layer, an erase gate generally placed on a second side of said floating gate separated therefrom by said second insulation layer, a drain region generally disposed on a first side of said floating gate, and a source region generally disposed on a second side of said floating gate.

10. A memory array as recited in claim 9 wherein said erase gate overlaps said floating gate and said control gate.

11. A method for fabricating a memory array comprising a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same rows are connected by a common word-line and the erase gates of the memory cells in the same columns

are connected by a common erase line, and the source regions of memory cells in the same rows are connected by a common source line, and drain regions of memory cells in the same columns are connected by a common drain lines, comprising the steps of :

a) providing a substrate;

b) defining a channel region;

c) growing field oxide in defined areas;

d) providing a first insulating layer;

e) depositing a first poly-silicon layer;

f) defining from said first poly-silicon layer a floating gate generally positioned over said channel region;

g) doping a source region;

h) providing a second insulating layer;

i) depositing a second poly-silicon layer;

j) defining a control gate and an erase gate; and

k) doping a drain region.

12. A method as recited in claim 11 wherein said control gate is generally positioned on a first side of said floating gate and overlapping said floating gate.

13. A method as recited in claim 11 wherein said erase gate is generally positioned on a second side of said floating gate and overlapping said floating gate.

14. A method as recited in claim 13 wherein said erase gate is generally positioned on said second side of said floating gate and overlapping said floating gate and said control gate.

15. A method as recited in claim 13 wherein said erase gate is generally positioned on said second side of said floating gate and overlapping said floating gate and about flush with said control gate.

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